Performance and Variability Studies of InGaAs Gate-all-Around Nanowire MOSFETs

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(Invited Paper)

***Abstract*—Furthering Si CMOS scaling requires development of high-mobility channel materials and advanced device structures to improve the electrostatic control. We demonstrate the fabrication of gate-all-around (GAA) indium gallium arsenide (InGaAs) MOSFETs with highly scaled atomic-layer-deposited gate dielectrics. InGaAs, with its high electron mobility, allows higher drive currents and other on-state performance compared to silicon. The GAA structure provides superior electrostatic control of the MOSFET channel with outstanding off-state performance. A subthreshold slope of 72 mV/dec, electron mobility of 764 $cm^2/V \cdot s$, and an on-current of 1.59 mA/μm are demonstrated, for example. Variability studies on on-state and off-state performances caused by the number of nanowire channels are also presented.**

***Index Terms*—Gate-all-around, InGaAs, MOSFET, nanowire.**

I. Introduction

III–V COMPOUND semiconductors has recently drawn wide interest in the device community for its potential application in future CMOS technology as channel materials [1]. Among various III–V materials under consideration, indium gallium arsenide (InGaAs) is considered one of the most promising materials for N-channel MOSFETs, due to its high electron mobility, high electron velocity, and unique band alignment. Various high-k dielectric integration schemes and interface passivation techniques have been investigated to improve high-k/InGaAs interface quality and achieve sub-1-nm equivalent oxide thickness (EOT) [2]–[7]. On the other hand, to meet the scaling requirements at sub-10-nm technology node, non-traditional device structure such as ultra-thin body and multiple-gate structure is strongly needed. Indium-rich InGaAs materials intrinsically have smaller bandgap, larger permittivity, and smaller effective mass, which make them even more susceptible to short channel effects. A III–V on-insulator structure with an extremely thin ($<$ 10 nm) body thickness has been demonstrated by wafer-bonding technique [8] and epitaxial transfer method [9]. In the meantime, InGaAs FinFETs with surface and buried channel have been proposed and demonstrated. Improved scalability has been confirmed with FinFET structure against planar and thin-body structure [10]–[12]. In the category of multiple gate devices, the gate-all-around (GAA) nanowire (NW) MOSFETs are the most promising option in terms of electrostatic control. High performance Si GAA NW devices have been demonstrated and its operating principle studied comprehensively [13]–[18]. Recently, a novel top-down fabrication technology has been developed and sub-50-nm InGaAs GAA NW MOSFETs have been demonstrated [4], [7], [19]. Scalability and variability improvements have been obtained by aggressive EOT scaling and interface passivation [20]. In this paper, the device performance for InGaAs GAA NW MOSFETs with various gate stack, NW size, and interface passivation has been summarized, with a particular focus on device variation aspects. This paper is organized as follows. Section II provides details of fabrication process and summarizes different samples under investigation. Sections III and IV study the channel length ($L_{\rm ch}$), NW size, and interface dependency for device on-state and off-state performance, respectively. Section V describes intrinsic device parameters, including the effective channel mobility. Section VI describes the unique variability induced performance shift in NW transistors.

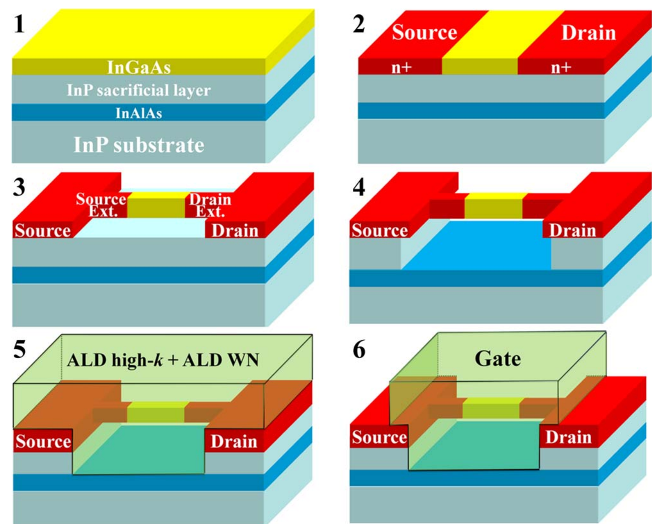

Fig. 1. Schematic view and key fabrication processes for InGaAs GAA FETs.

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TABLE I
FABRICATED AND CHARACTERIZED SAMPLES SUMMARY

Sample	Channel material	L_{ch} (nm)	W_{NW} (nm)	T_{NW} (nm)	Gate oxide	EOT (nm)	No. of wires
IEDM11	$In_{0.53}Ga_{0.47}As$	50-120	30-50	30	10nm Al_2O_3	4.5	1, 4, 9, 19
IEDM2012 (Sample A Al_2O_3-first)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	0.5nm Al_2O_3/ 4nm $LaAlO_3$	1.2	4
IEDM2012 (Sample B $LaAlO_3$-first)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	4nm $LaAlO_3$/ 0.5nm Al_2O_3	1.2	4
IEDM2012 (Sample C)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	3.5nm Al_2O_3	1.7	4
InGaAs GAA MOSFET (Unpublished Work)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	5nm Al_2O_3	2.2	4
Ultrathin InGaAs GAA MOSFET	$In_{0.65}Ga_{0.35}As$	20-80	20-30	6	5nm Al_2O_3	2.2	4

II. DEVICE FABRICATION

Fig. 1 shows a schematic view and the key fabrication processes for InGaAs GAA FETs. The starting material is InGaAs channel layers on a (100) InP substrate (Fig. 1-1). After $(NH_4)OH$ pretreatment, a 10 nm atomic-layer-deposited (ALD) Al_2O_3 was deposited as an encapsulation layer. Source/drain implantation (Si: $20\text{keV}/1 \times 10^{14}\text{cm}^{-2}$) was then performed, using PMMA resist as mask. The smallest channel length L_{ch} defined was 20 nm (Fig. 1-2). Dopant activation was done by rapid thermal annealing at 600 °C for 15 s in N_2 ambient. Then InGaAs fin structures were defined by ICP plasma etching (BCl_3/Ar) (Fig. 1-3). The diluted ZEP520A resist (100 nm) was used as etching mask. The smallest NW width (W_{NW}) defined was 20 nm. Then a localized NW release process was carried out using diluted HCl solution (Fig. 1-4). HCl based solution can selectively etch InP over InGaAs. However, the etching is found to be highly anisotropic. Therefore the InGaAs fins have to be patterned along $\langle 100 \rangle$ directions for a successful release process. After BOE and diluted HCl:H_2O_2 clean, the samples were soaked in 10% $(NH_4)_2S$ for 10 min. Then a high-k dielectric/WN metal gate was grown by ALD surrounding the NW channel as gate stack (Fig. 1-5). WN was grown at a temperature of 385 °C. Bis(tert-butylimido)bis(dimethylamido)tungsten(VI) vapor and ammonia gas were use as the WN precursors. The sheet resistance of the ALD WN film was measured by a four-point probe station, and the resistivity was 2.2 $\Omega \cdot$ cm for a 40 nm WN film. Cr/Au gate patterns were then defined and used as hard mask for the following gate etch using CF_4/Ar ICP plasma etching. The gate pattern has a 50 nm overlap region over the source/drain implanted area beyond the NW, as shown in Fig. 1-6, due to the non-self-aligned process. Source/drain metal was then formed by e-beam evaporation of Au/Ge/Ni and annealing at 350 °C. Cr/Au test pad definition concludes the fabrication process (Fig. 1-6). Table I summarizes the samples fabricated and characterized in this paper.

III. ON-STATE PERFORMANCE OF THE InGaAs GAA MOSFET

In this section, we discuss the key factors in the on-state performance of the InGaAs GAA MOSFETs. We have demonstrated three ways to improve the on-state performance of InGaAs MOSFETs: channel length, NW dimension, and EOT scaling.

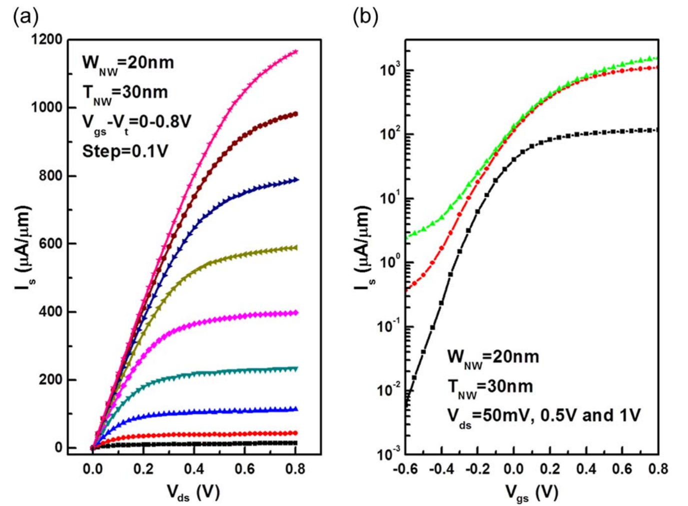

Fig. 2. (a) Output and (b) transfer characteristics of the device with the largest saturation source current 1.59 mA/μm at $V_{\text{ds}} = 1$ V.

A. Channel Length Scaling

The InGaAs GAA MOSFET has excellent immunity to short channel effect which enables us to continue the channel length scaling down to 20 nm. The extremely short channel enables us to obtain saturation current as high as 1.59 mA/mm at $V_{\text{ds}} = 1$ V in an InGaAs GAA MOSFET with a 20 nm channel length, a 20 nm wire width, a 30 nm wire thickness, and a 1.7 nm EOT. Fig. 2 shows the well-behaved output and transfer characteristics of this deep sub-100-nm NW device.

Channel length scaling is an effective way to improve the on-current in long channel devices because the saturation current is inversely proportional to the channel length. However, with the channel length step into sub-100-nm regime, I_{on} scaling saturates. Fig. 3 shows the on-current scaling metrics of the InGaAs GAA MOSFETs with different gate stacks. Samples A and B have a 0.5 nm Al_2O_3/4 nm $LaAlO_3$ stack $(\text{EOT} = 1.2\text{ nm})$, where Al_2O_3 was grown before $LaAlO_3$ for Sample A and vice versa for Sample B. Sample C has 3.5 nm Al_2O_3 gate $(\text{EOT} = 1.7\text{ nm})$. The saturation current increases very slowly

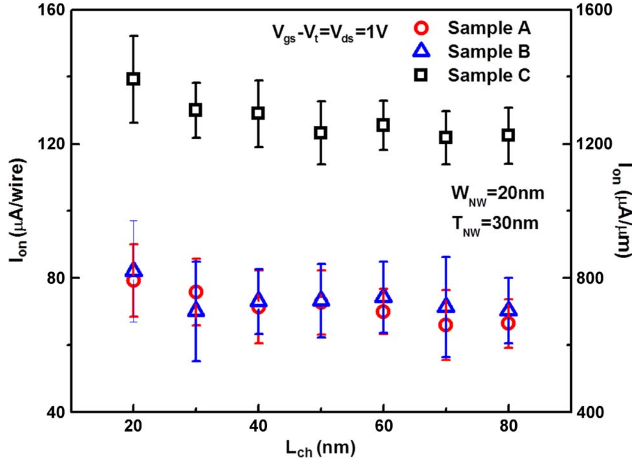

Fig. 3. I_{on} scaling metrics of InGaAs GAA MOSFETs with three gate stacks.

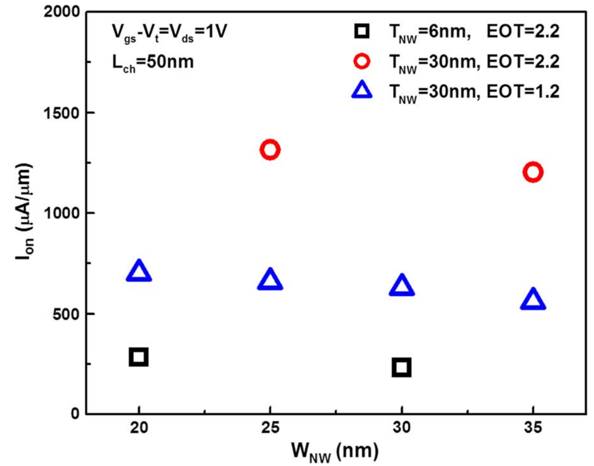

Fig. 4. Effect of NW dimension W_{NW} on the on-current.

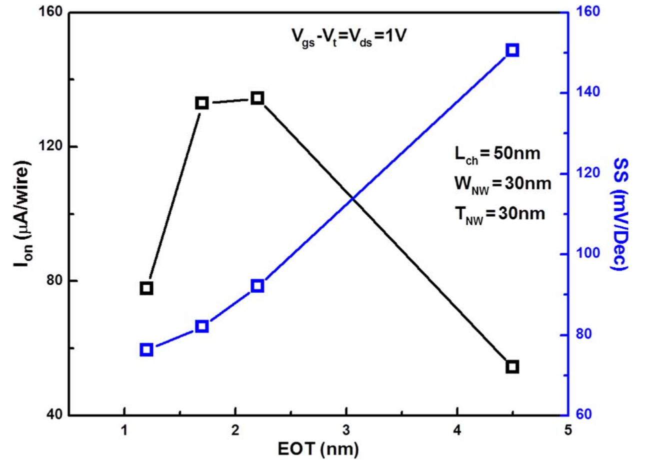

Fig. 5. Effect of EOT scaling on the on-currents of different devices.

in the sub-100-nm regime by decreasing channel length. The reasons are twofold: On the one hand, velocity saturation limits the velocity of the electron at high electric field [21]. In short channel devices, the strength of the electrical field is so high that the velocity of electron almost stays the same with different channel lengths so as to the saturation current. On the other hand, statistical law in electron transportation does not work in extremely short channel devices. The short channel devices may work in a near ballistic regime. The electron in the channel is likely to transport from source to drain without scattering or only scatter for a few times. In this case, the current of the device depends more on the contact of the transistor rather than the channel length. When totally ballistic transport is obtained, the current only depends on the contact resistance [22].

B. NW Dimension Optimization

An InGaAs GAA MOSFET has a relatively larger drive current, compared to other device structures such as planar structure and FinFET structure because of the better gate control. Simulation works have shown that the channels of InGaAs GAA MOSFETs are volume inverted, which explains the fact that devices with smaller NW structures show larger normalized on-current [23].

We have systematically studied the dimension dependency of the on-currents. Devices with a 20–35 nm NW width (W_{NW}) and a 6 nm or a 30 nm NW thickness were fabricated, and the dependence of on-current with the geometrical dimension of the transistor is presented in Fig. 4. It is found that the on-current keeps increasing with NW dimension scaling from 35 to 20 nm, consistent with simulation work. However, devices with a 6 nm NW thickness have relatively low current. The reason is that surface roughness has more significant effect on the mobility of the InGaAs channel than volume inversion when the channel is down to 6 nm level. Because the NW is so thin, electrons are more likely to scatter at the surfaces, and mobility is degraded.

C. EOT Scaling

It is well known that the on-current of a MOSFET is proportional to the gate capacitance (C_{ox}) at the same drain and gate biases and that C_{ox} is inversely proportional to the equivalent gate oxide thickness (EOT). Thus, it is an effective way to improve the on-current at the same bias conditions by scaling EOT.

Here, InGaAs GAA MOSFETs with EOT = 4.5 nm (10 nm Al_2O_3), EOT = 2.2 (5 nm Al_2O_3), EOT = 1.7 (3.5 nm Al_2O_3), and EOT = 1.2 (0.5 nm Al_2O_3/4 nm $LaAlO_3$) are used to compare the on-current with different EOTs. Fig. 5 shows the relationship between the on-current and the EOT. Theoretically, I_{on} and EOT should form a straight line in the plot. However, we found that the curve resembles a parabola with a peak at around 2 nm. The reason is that with EOT scaling down, remote scattering from the oxide layer such as Coulomb scattering, becomes larger. Therefore, the mobility of devices with a smaller EOT is degraded, compared to a larger EOT device [24]. As a result, the currents of the devices with an EOT less than 2 nm are decreased.

IV. Off-State Performance of the InGaAs GAA MOSFET

One of the scalability bottlenecks of planar MOSFETs is the short channel effect. Excellent immunity to short channel effect is another benefit of the InGaAs GAA MOSFETs. In

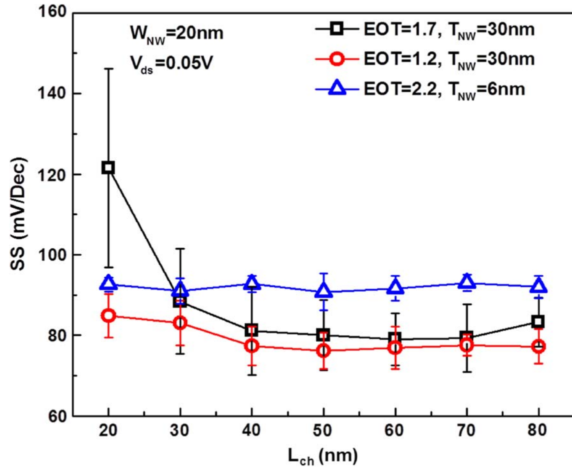

Fig. 6. SS channel length scaling metrics for different EOT and NW dimensions.

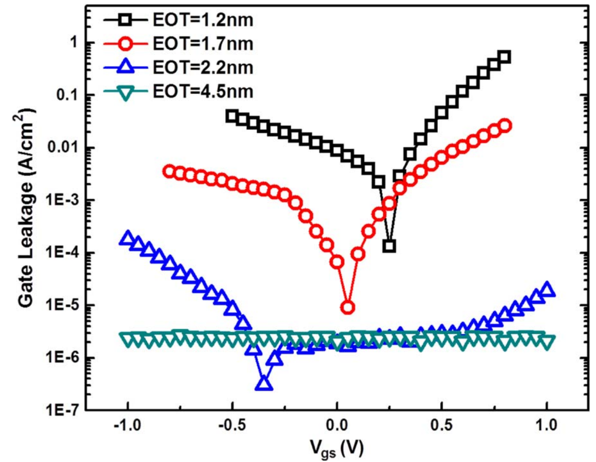

Fig. 7. Relationship between EOT and gate leakage current.

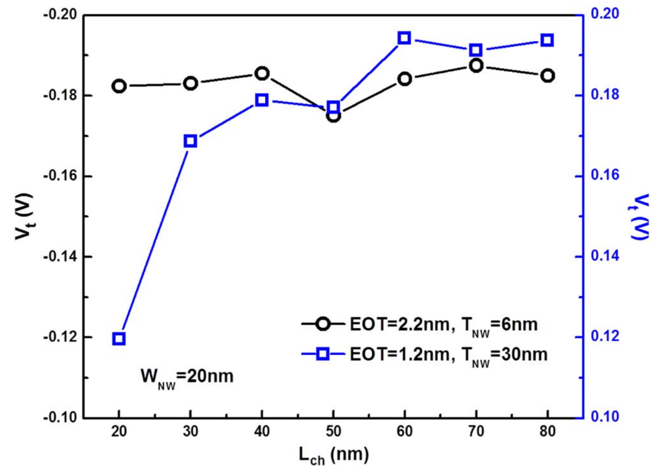

Fig. 8. Channel length scaling metrics for threshold voltage.

this section, we mainly focus on the experimental evidence on how significant the GAA structure can reduce the short channel effect of the InGaAs MOSFETs. Generally, there are three ways to improve the off-state performance: EOT scaling, NW dimension shrinkage, and interface engineering.

A. EOT Scaling

One of the most straightforward ways to improve the off-state performance is to reduce the EOT. Lower EOT leads to better electrostatic control and in turn, smaller SS and drain-induced barrier lowering (DIBL). Fig. 5 shows the relationship between EOT and SS using devices with $L_{\text{ch}} = 50$ nm, $W_{\text{NW}} = 30$ nm, and $T_{\text{NW}} = 30$ nm. We can see clearly that devices with lower EOT have better off-state performance. Fig. 6 shows the comparison of SS between two groups of devices with EOT $=$ 1.2 nm, EOT $=$ 1.7 nm, and 30 nm wire thickness. We can find that devices with EOT $=$ 1.2 nm have a much smaller SS and almost no increase with channel length scaling down to 20 nm.

We have seen that EOT scaling is an effective way to improve the off-state performance. However, keeping push EOT down to 1 nm or less is still challenging. Fig. 7 shows the relation between gate leakage current and EOT. Leakage current increases very fast with EOT scaling down. Theoretically, the gate leakage current has an exponential relationship with the gate insulator thickness. That is why high-k material (LaAlO_3, $k \sim 25$) is used in this work. As described in the previous section, carrier mobility in the channel could also be degraded with aggressively scaled EOT.

B. NW Dimension Scaling

Another way to improve the off-state performance is to reduce the dimension of the NW so that better gate control can be achieved. As shown in Fig. 6, the devices with EOT $=$ 2.2 nm and 6 nm thick NW show no SS increase with channel length scaling, which means that the ultrathin device has better immunity to short channel effect. Meanwhile, the devices with EOT $=$ 1.2 nm and 1.7 nm and $T_{\text{NW}} = 30$ nm show the increase of SS when the channel is 40 nm or less.

As shown in Fig. 6, the device with $T_{\text{NW}} = 6$ nm shows the largest SS in the long channel regime. The reason is that SS not only depends on the immunity to short channel effect but also on the interface trap density (D_{it}). Without taking short channel effect into account, the SS can be expressed as SS $= 60(1 + qD_{\text{it}}/C_{\text{ox}})$. The higher the D_{it} is, the larger the SS. By EOT scaling, C_{ox} can be increased, and therefore, the effect of interface trap on SS is reduced.

Fig. 8 shows the V_t comparison between the device with EOT $=$ 2.2 nm and $T_{\text{NW}} = 6$ nm and the device with EOT $=$ 1.2 nm and $T_{\text{NW}} = 30$ nm; both of them have the same NW width, and a linear extrapolation method is used in V_t extraction. It can be seen clearly that V_t rolls off in device with EOT $=$ 1.2 nm and $T_{\text{NW}} = 30$ nm; however, V_t remains the same in device with EOT $=$ 2.2 nm and $T_{\text{NW}} = 6$ nm. The V_t roll-off verifies that those devices with EOT $=$ 1.2 nm and $T_{\text{NW}} = 30$ nm are still strongly affected by the short channel effect at channel length of 50 nm or less, whereas the ultrathin 6 nm NW devices have better immunity to short channel effect.

Therefore, in short channel InGaAs NW devices, both interface trap and short channel effects can degrade the off-state

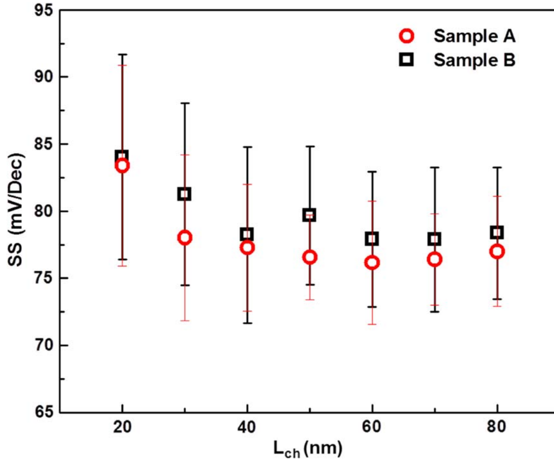

Fig. 9. SS comparison between devices with different gate stack at EOT = 1.2 nm, $T_{\rm NW} = 30$ nm and $W_{\rm NW} = 20$ nm. Samples A and B have a 0.5 nm Al_2O_3/4 nm $LaAlO_3$ stack (EOT = 1.2 nm), where Al_2O_3 was grown before $LaAlO_3$ for sample A and vice versa for sample B. Sample A has a better interface than Sample B.

performance. EOT scaling improves the off-state performance by providing better gate control and reducing the effect of $D_{\rm it}$ with increased gate capacitance. On the other hand, the NW dimension scaling can improve the off-state performance only by providing better gate control to reduce the short channel effect. The ultrathin NW structure gives a better immunity to short channel effect than EOT scaling.

C. Interface Engineering

Interface trap density is one of the factors that degrade the off-state performance as discussed above. Fig. 9 compares devices with different gate stack, thus with different $D_{\rm it}$. We found that the 0.5 nm Al_2O_3/4 nm $LaAlO_3$ stack has a lower average SS than the 4 nm $LaAlO_3$/0.5 nm Al_2O_3 stack. Thus, it is confirmed that a better interface quality can be obtained with thin Al_2O_3 layer insertion between high-k $LaAlO_3$ and InGaAs.

V. Effective Mobility

The on-state performance of a device is strongly correlated to the mobility of the channel semiconductor. Although electron mobility (μ_n) of bulk InGaAs is $\sim 10^4$ cm^2/V $\cdot$ s, the mobility is reduced considerably for a fully processed GAA transistor, due to non-ideal effects such as series resistance and interface scattering. These effects must be de-embedded from measured data in order to determine the true performance of the InGaAs GAA MOSFET.

Here, we pursue for extraction of intrinsic effective mobility of InGaAs NW channels by fitting measured data to a MOSFET model based on the BSIM3 Unified I–V Model [25]. The BSIM model does not fit the NW characteristics in the deep-subthreshold region where drain to source leakage has a significant effect. An extra drain to source leakage term, $I_{{\rm leak},V_{\rm ds}}$, is added to the model. Since the magnitude of leakage is dependent on the drain voltage, its value must be extracted for each $V_{\rm ds}$ measured. With this extra parameter, the model fits the NWs in the low $V_{\rm ds}$ region ($V_{\rm ds} \lesssim 2v_t$) very well, even though it was designed for planar silicon devices.

The core of the low-$V_{\rm ds}$ model is a formula for an effective gate to source voltage ($V_{\rm gsteff}$):

$$V_{\rm gsteff} := \frac{2nv_t \ln\left[1+\exp\left(\frac{V'_{\rm gs}-V_t}{2nv_t}\right)\right]}{1+2nC_{\rm ox}\frac{v_t}{Q_0}\exp\left(-\frac{V'_{\rm gs}-V_t}{2nv_t}\right)}$$

where n is the subthreshold swing parameter, v_t is the thermal voltage kT/q, $V'_{\rm gs}$ is the intrinsic gate voltage and equals $V_{\rm gs} - I_sR_s$, R_s is assumed to be half of series resistance $R_{\rm ds}$, V_t is the threshold voltage and is dependent on $V_{\rm ds}$ because of short channel effects, $C_{\rm ox}$ is the gate to channel capacitance, and Q_0 is the charge in the channel at threshold [25].

The use of $V_{\rm gsteff}$ allows a simple equation to be used for calculating the device current in both the subthreshold and strong inversion regions. $V_{\rm gsteff}$ is approximately $(V_{\rm gs} - V_t)$ in the strong inversion region and $(Q_0/C_{\rm ox})\exp[(V'_{\rm gs} - V_t)/nv_t]$ in the subthreshold region. Incorporating $I_{{\rm leak},V_{\rm ds}}$ and $R_{\rm SD}$ allows the following to be used to implicitly solve for I_S:

$$I_S = \frac{W}{L}\mu C_{\rm ox}V_{\rm gsteff}(V_{\rm ds} + I_SR_{\rm SD}).$$

W is the device width, L is the channel length, and I_S is the source current [25]. The device width is taken to be the circumference of the wires, and $C_{\rm ox}$ is calculated based on the oxide material and its thickness.

The device mobility μ is modeled as

$$\mu := \frac{\mu_0}{1+\theta_1(V_{\rm gsteff})+\theta_2(V_{\rm gsteff})^2}.$$

This formula describes how increasing the gate to channel electric field causes the mobility to decrease, e.g., because of increasing interface scattering. We model this effect by using a first and second order correction term to model the changes of mobility as a function of $V_{\rm gsteff}$ so that this correction term can be included when the device is operated in the subthreshold region.

Methodology A: The parameter extraction is made difficult because two device parameters exist that have nearly identical effects on the on-state performance: the mobility degradation factor θ_1 and the device series resistance $R_{\rm SD}$. Both effects are dependent on the applied $V_{\rm gs}$. If the change in $V_{\rm gs}$ due to the voltage drop over the series source resistance is not taken into account, then they are interchangeable model parameters and related by $\theta_1 \Leftrightarrow (W/L)\mu_0R_{\rm SD}$.

One way to separate these two effects is to measure a series of devices with various channel lengths that are otherwise identical [26]. A linear extrapolation can be made to determine the series resistance of a “zero-length” device. This is problematic for the GAA InGaAs devices for two reasons: device variability and the influence of short channel effects.

The GAA InGaAs NW devices have significant variation in not only $R_{\rm SD}$ but also other device parameters (e.g., subthreshold slope and V_t, as shown in Figs. 13 and 14). These variations cause the extrapolation to be unreliable.

If short channel effects (e.g., threshold voltage shift and DIBL) are significant, then the relationship between the apparent $R_{\rm SD}$ (setting θ_1 to be zero) and the channel length will become non-linear, making it difficult to estimate the value at zero length.

Methodology B: An alternative method to determine $R_{\rm SD}$ is to perform $I_D{-}V_G$ measurements at multiple $V_{\rm DS}$ biases [27]. This method has the advantage that it only requires measurements from a single device, and as such, any variation between devices is irrelevant to the extraction. Also, it is resistant to short-channel effects because it only relies on low $V_{\rm ds}$ biases where short channel effects (if present) can be neglected.

As presented, this method compares the current at various $V_{\rm ds}$ biases at a fixed $(V_{\rm gs} - V_t)$. Because of the low $V_{\rm ds}$ assumption and the equal gate biases, the mobility will be equal within each set of data. When using the square-law MOSFET model, the ratio of the currents can be analyzed and gives a value that is independent of the mobility. The series resistance can be solved for in the following case:

$$\frac{I_{D1}}{I_{D2}} = \frac{(V_{\rm gs1} - V_{t1} - I_{d1}R_{\rm SD}/2)(V_{D1} - I_{D1}R_{\rm SD})}{(V_{\rm gs2} - V_{t2} - I_{d2}R_{\rm SD}/2)(V_{D2} - I_{D2}R_{\rm SD})}.$$

The threshold voltages can be extracted via the Y-function method [26], neglecting θ_2, by examining the Y-intercept of

$$Y := \frac{I_D}{\sqrt{g_m}} \approx \sqrt{\mu_0 C_{\rm ox}\frac{W}{L}V_{\rm ds}}(V_{\rm gs} - V_t).$$

By determining the value $R_{\rm SD}$ using this extraction method and then fitting the measured data to the MOSFET model, the intrinsic device parameters can be determined. A non-linear solver is used to optimize the model parameters to best fit the measurement data.

As an example of this method, an array of four 30 nm × 30 nm NWs with a gate length of 120 nm and an Al_2O_3 gate dielectric with EOT = 4.5 nm was measured. It was found to have a series resistance of 5503 Ω. The range in threshold voltage was −0.325 to −0.295 V from $V_{\rm ds} = 5$ to 100 mV, respectively, confirming that short-channel effects are minimal and that the low-$V_{\rm ds}$ assumption is valid. The mobility $\mu_0 = 764\ {\rm cm}^2/{\rm V\cdot s}$, while θ_1 is 0.11/V. Similar to in Silicon NW devices [26], θ_2 is negligible and is approximately $0.060/{\rm V}^2$ for this InGaAs device. Output of these model parameters is shown in Fig. 10. The closeness of the modeled lines with the measured data for linear and log scale I_s, along with the transconductance g_m, demonstrates the validity of the model. The mobility parameters θ_1 and θ_2 model how the mobility decreases as the gate voltage increases, as shown in Fig. 11. The mobility decreases to $713\ {\rm cm}^2/{\rm V\cdot s}$ when I_s is 90% of its maximum ($V_{\rm gs} = 0.3$ V).

VI. Variability Induced Performance Drift

As the traditional devices scale down, the variability among transistors on a chip becomes prominent due to reasons such as random dopant fluctuation, random telegraphic noise, process variation, etc. [28]–[30]. However, since the transistors based on NWs typically have several NWs in parallel, there is an additional source of variability arising from the transport characteristics of different NWs within a single transistor. As we will see, this sometimes leads to a systematic drift to the device performance as a function of the number of (parallel) NWs within a given transistor. In this section, we will discuss how this NW-to-NW variability affects on-state and off-state parameters.

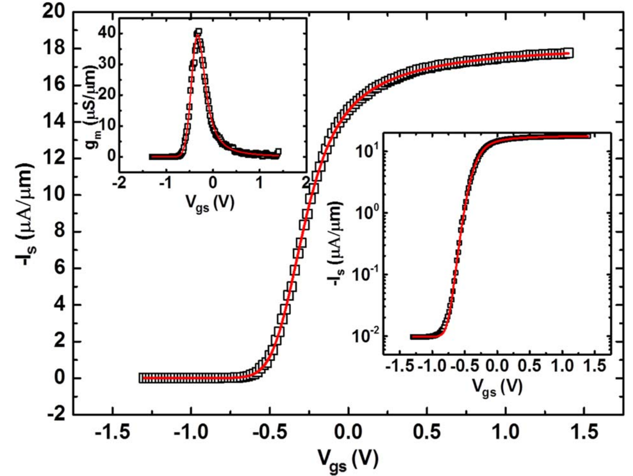

Fig. 10. Data from an array of four 30 × 30 NWs measured at $V_{\rm ds} = 50$ mV, linear scale with an inlay of log scale I_s and linear scale g_m. Symbols are measured data points, and lines are calculated based on the model parameters.

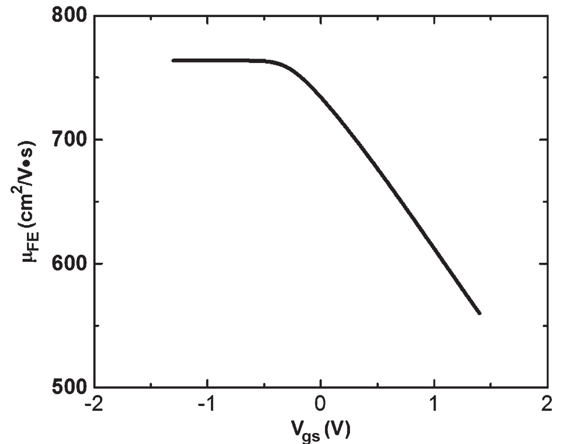

Fig. 11. Field effect mobility changes with $V_{\rm gs}$ in an array of four 30 × 30 NW devices.

A. On-State Performance

We have seen in Section III that how the on-current $(I_{\rm ON})$ of a GAA MOSFET depends on channel length, NW dimension, and EOT. However, for a given set of such parameters, one would expect that $I_{\rm ON}$ should increase linearly with the number of parallel NWs. For example, for a single NW transistor, the total on-current $I_{{\rm ON},1} \sim V_{\rm ds}/(R_{\rm ch} + R_{\rm SD})$, where $V_{\rm SD}$ is the drain voltage, $R_{\rm ch}$ is the channel resistance at the given condition, $R_{\rm SD}$ is the source–drain series resistance. For n number of NWs in parallel, the expected total on-current is $I_{{\rm ON},n} \sim V_{\rm ds}/(R_{\rm ch}/n + R_{\rm SD}/n) = n \times I_{{\rm ON},1}$, assuming that the total R_S is constant, and consequently, the series resistance

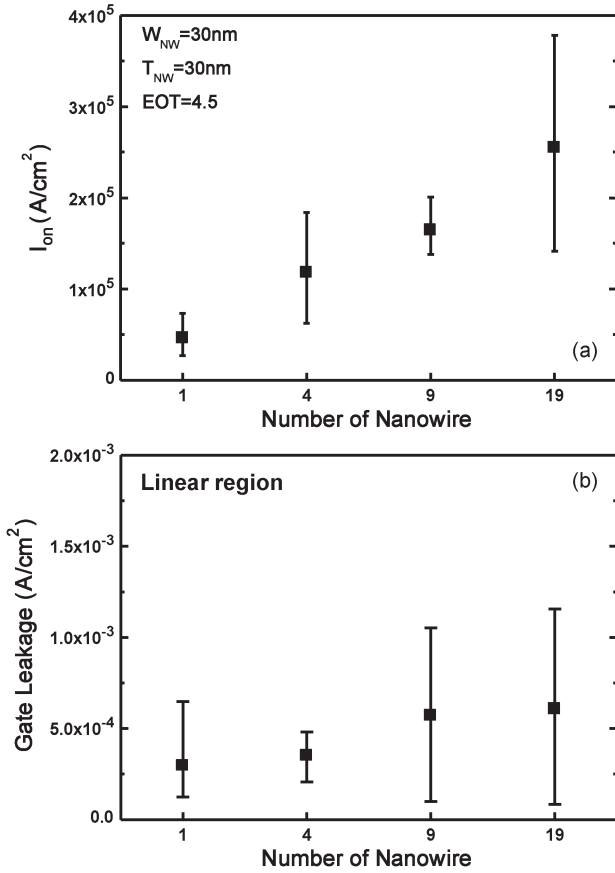

Fig. 12. (a) The on current density as a function of the number of parallel NWs in a given transistor. Contrary to the planner devices, the current density increases with increasing the number of NWs, or equivalently increasing the channel area. (b) The gate leakage density remains relatively unchanged with the number of NWs, as expected, for the same set of devices.

per NW is decreased with the increase of the number NWs. Ideally, therefore, the *current density* (averaged over the total cross sectional area of all the NWs) should remain constant regardless of the number of NWs. Fig. 12(a) shows the average I_{ON} (A/cm^2) as a function of the number of NWs in a given transistor. In this measurement, the width and thickness of each NW is 30 nm, and EOT $= 4.5$ nm. Clearly, $I_{\mathrm{on}}(\equiv I_{\mathrm{ON},n}/n)$ is not constant; rather, it increases as the number of NW increases. This implies that the series resistance per NW decreases super-linearly (i.e., smaller than R_{SD}/n) with the number of NWs. Equivalently, the total R_S actually decreases with the increase of the NWs. One might imagine the possibility of lesser current crowding for more number of NWs leading to lower contact resistance [31]. However, further work is required for exact origin of such dependence of R_{SD} (and hence I_{ON}) on the number of NWs.

For the same set of devices, the average gate leakage currents do not vary significantly with the number of NWs [Fig. 12(b)], confirming that the NW dimensions are identical and the increase of I_{ON} in Fig. 12(a) cannot be attributed to process induced artifacts associated with increasing number of NWs.

B. Off-State Performance

It has been discussed in Section IV that the sub-threshold slope of the GAA InGaAs transistor could traditionally degrade

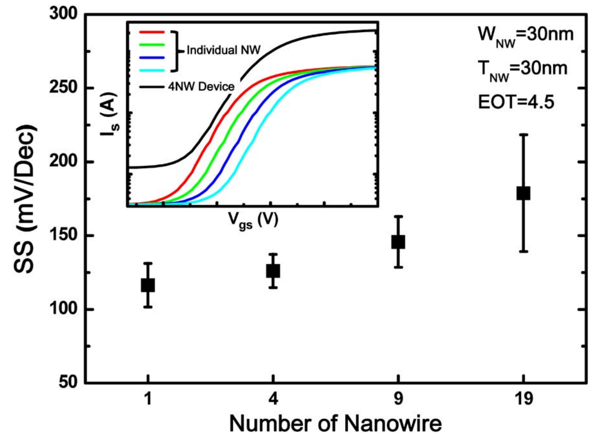

Fig. 13. SS as a function of the number of NWs shows performance degradation as the number of NW increases.

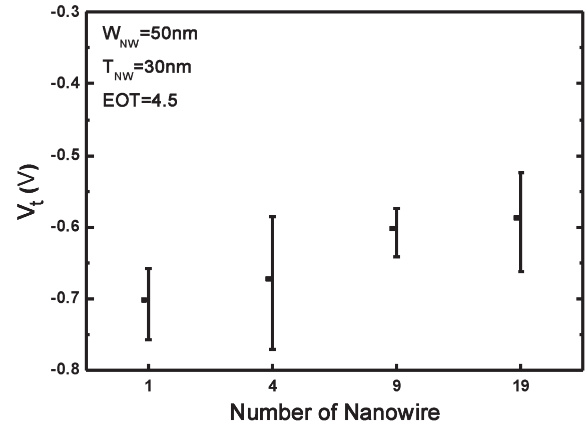

Fig. 14. V_t increases with the number of NW increases, possibly due to the self-heating effect and worse heat dissipation for higher number of parallel NWs.

due to short channel effect as well as the interface defects. Here we show another variability-induced SS degradation in the GAA transistors. Fig. 13 shows the SS measurements on the same set of devices as used in this section. The result shows more than 50% increase in SS as the number of NWs increases from 1 to 19. This could be explained from the V_t variation within NWs in a given transistor (Fig. 13, inset). With a given distribution of V_t, the NWs start turning on sequentially as the voltage increases, giving rise to a higher SS.

Finally, Fig. 14 shows an increase of V_t as a function of the number of NWs. The possible origin could lie on the self-heating effect, which increases the local temperature of the channel region during operation. Higher density of NWs in a given transistor makes heat dissipation difficult, and the corresponding higher temperature may increase activated trapping of carriers within the gate oxides [32]. Such temperature-dependent trapping may increase V_t as a function of the number of NWs in a given transistor.

VII. Conclusion

InGaAs GAA NW MOSFETs offer a path towards the further scaling of transistors for ultimate CMOS technology

development. They provide superior electrostatic control of the device channel, allowing higher on-current and lower SS and DIBL. We demonstrate various InGaAs NW MOSFETs using ALD gate dielectrics with EOT as low as 1.2 nm and electron mobility of 764 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ in the channel. Device performance and variability are examined experimentally with the trends associated with the device dimensions, EOT, and interface quality.

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